UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/528,001	03/17/2000	Shiri Kadambi	P108339-00003	3385

32294 7590 06/28/2004

SQUIRE, SANDERS & DEMPSEY L.L.P.
14TH FLOOR
8000 TOWERS CRESCENT
TYSONS CORNER, VA 22182

EXAMINER	
HOANG, THAI D	

ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/528,001	KADAMBI ET AL.	
	Examiner	Art Unit	
	Thai D Hoang	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment filed on 04/09/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, lines 13-14, the statement "module headers having module identifier fields" is confusing. According to the specification in pages 102-103, the module header does not have "module identifier fields". Instead, it only has "MT Module Id Bitmap" field (p. 102, lines 24-27) and "Module Id Bitmap" field (p. 103, lines 4-5),. Therefore, it is not clear the "module identifier fields" recited in claim 1 implies the "MT Module Id Bitmap" field or the "Module Id Bitmap" field as disclosed in the specification.

Claims 2-6 are rejected because they depend on rejected claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 are rejected under 35 U.S.C. 102(a) as being unpatentable over Muller et al, US patent No. 5,909,686, in view of Fine et al., US Patent No. 6,188,694 B1 hereafter referred to as Muller and Fine respectively.

Regarding claim 1, as best understood, Muller discloses a network switch stack configuration, which comprises a plurality of switching elements 100, wherein each of elements 100 comprises a plurality of data ports located at network interface 205, a cascading interface 225 and a CPU interface 215; see figures 1-2; col. 3, lines 39-41; col. 4, lines 38-43 (a first network switch comprising a plurality of data ports, a first stacking port, and a first CPU interface; a second network switch having a plurality of data ports, a second stacking port, and a second CPU interface). In addition, Muller teaches that the network comprises a common CPU 161 connected to each of the interfaces 215 of the switching elements 100 (a common CPU connected to said first CPU interface and said second CPU interface). Muller discloses that the switching elements 100 of subsystems 110 are interconnected to form of cascading as shown in figure 1 by using a number of links 141. Therefore, it indicates that incoming data packets are transmitted from one the data ports of the switching element 100 to any of the data ports of another switching element 100; figures 1-2; col. 4, lines 1-5, 44-57; col. 5, lines 10-21; col. 6, lines 6-30 (the first stacking port and the second stacking port are communicatively connected, such that incoming packets on any of the plurality of data ports on the first and second switches can be effectively switched to any of the plurality of data ports on either of the first and second network switches.) Each of the switch elements 100 in the system shown in figure 1 inherently add to each of the incoming

data packets a header for routing the data packets to a destination; and read the headers to determine egress port according to the information of the headers; col. 13, lines 9-22. Muller does not teach that the headers comprise "module identifier fields". However, Fine teaches a header that comprises "switch ID field" (fig. 3B, element 354). It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the switch ID field disclosed by Fine into Muller's method in order to control transmission of data packets in the network.

Regarding claim 2, Muller teaches that a central processing system (CPS) 160 that is coupled to the individual subsystem 110 through a communication bus 151. The CPS 160 has a direct control and communication interface to each subsystem 110 and provides some centralized communication and control between switch elements; col. 4, lines 24-34. Furthermore, Muller discloses that the CPU 161 may transmit commands or packets to the network switch element 100 via the CPU interface 215. In this manner, one or more software processes running on the CPU 161 may manage entries in an external forwarding and filtering database 140. It indicates that the CPU 161 is configured to program functions on the switching elements, and controls communication between switching elements (common CPU is configured to program functions on the first and second network switch, and wherein the common CPU controls communication between the first and second network switch.)

Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al, US patent No. 5,909,686, in view of Muller et al, US Patent No. 6,119,196, hereafter referred to as 686 and 196.

Regarding claims 3-5, 686 teaches that the switching elements 100 are interconnect in form of stack through interfaces 205 and 225 connected by a plurality of links 141. 686 does not teach that the cascading interface 225 includes an arbiter for allocating communication bandwidth between the first and second stacking port, and a flow control logic for controlling data flow to and from each of the first and second network switches. However, 196 teaches that a switch 100 comprises a cascading interface 108 connected with a shared memory manager 110 including a buffer memory controller (BMC) 112; see fig. 1. The BMC 112 comprises an arbiter 210 and an arbiter/scheduler 214 (see fig. 2) in order to allocate bandwidth and control data rate for fast ports 222 and slow ports 202. Therefore, it implies that the BMC 112 performs the functions as recited in claims 3-5. However, 196 does not teach that the BMC 112 located at the interfaces 106 and 108. *See In re Japikse, 86 USPQ 70 (CCPA 1950)*. It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the bandwidth allocating method disclosed by 196 into 686's system for utilizing the bandwidth of the system in order to maximize data transmission through the system.

Regarding claim 6, 686 does not disclose that the system forwards data packets to the egress ports without requiring a lookup in an address table. However, 196 discloses that the system comprises arbiters to determine output port based on an access request of the data packets, abstract, figs. 2-4; col. 1, line 57 – col. 2, line 6; col. 3, line 46 – col. 4, line 31. Therefore, it indicates that the system does not comprise a lookup table to determine output ports for the data packets. It would have been obvious

to one of ordinary skill in the art at the time the invention was made to adapt the method disclosed by 196 into 686's system in order to simplify for reducing the cost of the system.

Response to Arguments

Applicant's arguments with respect to claim 1 has been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai D Hoang whose telephone number is (703) 305-3232. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (703) 305-4378. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thai Hoang

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 6/25/04